

Application No. 10/681,517  
Amendment dated August 5, 2005  
Reply to Office Action of April 5, 2005

**Amendments To the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1           Claim 1 (currently amended): A phase control loop circuit for tuning to a  
2           reference frequency signal comprising:  
3                 a phase lock loop (PLL) circuit being responsive to a reference frequency  
4                 signal having a reference frequency, said PLL circuit including a voltage  
5                 control oscillator (VCO) for generating a VCO output, said PLL circuit for  
6                 generating a PLL output, said phase control loop circuit processing said  
7                 VCO output to generate an output frequency signal having an output  
8                 frequency; and  
9                 a coarse tuning circuit being coupled to said PLL circuit, said coarse  
10                tuning circuit being responsive to said PLL output for processing the same  
11                to generate a counter output, said VCO being responsive to said counter  
12                output, said counter output being used for coarse tuning said output  
13                frequency signal to said reference frequency signal, said coarse tuning  
14                circuit further responsive to a lock detection (LD) signal, said LD signal  
15                for controlling said counter output to cause said output frequency to be  
16                within a predetermined range of frequencies including said reference  
17                frequency, said PLL circuit for fine tuning said output frequency signal to  
18                said reference frequency signal,  
19                wherein said PLL circuit and said coarse tuning circuit tune the output  
20                frequency to [a] the reference frequency included in a wide range of  
21                frequencies further wherein said PLL circuit includes a phase-frequency  
22                detector (PFD) circuit for comparing said output frequency with said  
23                reference frequency to generate a PFD output, said PFD output including a

24            $\Delta f$  signal for representing the difference between said output frequency  
25           and said reference frequency, said PLL circuit further including a charge  
26           pump (CP) circuit responsive to said PFD output for generating a current,  
27           the value of said current being based on the value of said  $\Delta f$  signal,  
28           wherein said PLL circuit further includes a loop filter responsive to said  
29           current for converting the same to generate a control voltage ( $V_{ctrl}$ ) signal  
30           having a voltage value  $V_{ctrl}$ , said  $V_{ctrl}$  signal being provided to said VCO  
31           to control said VCO output, said  $V_{ctrl}$  signal controlling said VCO output  
32           to enable said PLL circuit to fine tune said output frequency to said  
33           reference frequency, further wherein said coarse tuning circuit includes a  
34           comparator circuit, said comparator circuit including a first comparator  
35           and a second comparator, said  $V_{ctrl}$  signal being included in said PLL  
36           output, said first and second comparators being responsive to said PLL  
37           output, said first comparator being responsive to a first fixed value signal  
38           having a first voltage value, said second comparator being responsive to a  
39           second fixed value signal having a second voltage value.

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1           Claim 2 (canceled).

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1           Claim 3 (canceled).

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1           Claim 4 (canceled).

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1 Claim 5 (original): A phase control loop circuit as recited in claim 1 further  
2 including a divider circuit responsive to said VCO output for dividing the same by  
3 a factor N to generate said output frequency signal.

1 Claim 6 (canceled).

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1 Claim 7 (currently amended): A phase control loop circuit as recited in claim [6] 1  
2 wherein said first voltage value is two thirds of a predetermined voltage value  
3 ( $V_{cc}$ ), said second voltage value is one third of said  $V_{cc}$ .

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1 Claim 8 (original): A phase control loop circuit as recited in claim 7 wherein said  
2 first comparator for comparing said  $V_{ctrl}$  to said first voltage value, said second  
3 comparator for comparing said  $V_{ctrl}$  to said second voltage value, said first  
4 comparator for generating a first comparator output and said second comparator  
5 for generating a second comparator output.

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1 Claim 9 (original): A phase control loop circuit as recited in claim 8 wherein said  
2 coarse tuning circuit further includes a counter control circuit, said counter control  
3 circuit including a first nand gate and a second nand gate responsive to said first  
4 comparator output, said first nand gate being responsive to said second  
5 comparator output, said second nand gate being responsive to an inverted version  
6 of said second comparator output.

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1 Claim 10 (original): A phase control loop circuit as recited in claim 9 wherein  
2 said coarse tuning circuit further includes a counter for generating a counter  
3 output, the output of said first nand gate causes said counter to count, the output  
4 of said second nand gate causes said counter output to be maintained.

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1 Claim 11 (original): A phase control loop circuit as recited in claim 10 wherein  
2 said counter being responsive to the output of a third nand gate, said third nand  
3 gate being responsive to a lock detection (LD) signal and a clock signal, said  
4 clock signal provides clock cycles to said counter wherein at each said clock cycle  
5 said counter begins to count, said LD signal for overriding said clock signal to  
6 halt the counting performed by said counter.

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1 Claim 12 (original): A phase control loop circuit as recited in claim 8 wherein  
2 said VCO has a positive polarity, said  $V_{ctrl}$  being less than said second voltage  
3 value causes said counter to count up to increase said counter output, said  $V_{ctrl}$   
4 being greater than said first voltage value causes said counter to count down to  
5 decrease said counter output, said  $V_{ctrl}$  being greater than said second voltage  
6 value and less than said first voltage value causes said second counter to stop  
7 counting and maintain said counter output, said  $V_{ctrl}$  being greater than said  
8 second voltage value and less than said first voltage value causes said output  
9 frequency to be within said predetermined range of frequencies.

1 Claim 13 (original): A phase loop control circuit as recited in claim 10 wherein  
2 said counter is a 4-bit counter, said counter enabling said phase control loop  
3 circuit to tune said output frequency to said reference frequency included in an  
4 increased range of frequencies.

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1 Claim 14 (currently amended): A phase control loop circuit as recited in claim 1  
2 [included within a receiver for receiving] responsive to radio frequency (RF)  
3 [signals,] signals [said receiver further including a low noise amplifier responsive  
4 to said RF signals] for use in generating amplified RF signals for use by a mixer[,  
5 said receiver further including a mixer responsive to said amplified RF signals  
6 and said VCO output] for converting said amplified RF signals to baseband  
7 signals.

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1 Claim 15 (original): A phase control loop circuit as recited in claim 11 wherein  
2 said PLL circuit is essentially an analog circuit, said LD signal for preventing  
3 jitter generated by said comparator circuit to affect said PLL circuit.

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1 Claim 16 (original): A phase control loop circuit as recited in claim 14 for tuning  
2 to said reference frequency included in a wide range of frequencies to compensate  
3 for the process variations caused by manufacturing said receiver.

1 Claim 17 (original): A phase control loop circuit as recited in claim 1 wherein  
2 said PLL circuit and said coarse tuning circuit cause said output frequency signal  
3 to have essentially the same phase as said reference frequency signal.

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1 Claim 18 (original): A phase control loop circuit as recited in claim 1 wherein  
2 said PLL circuit and said coarse tuning circuit tune said output frequency to said  
3 reference frequency on-the-fly.

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1 Claim 19 (currently amended): A method for tuning to a reference frequency  
2 signal comprising:  
3 receiving the reference frequency signal having a reference frequency;  
4 generating a voltage control oscillator (VCO) output;  
5 generating a phase lock loop (PLL) output;  
6 processing the VCO output to generate an output frequency signal having an  
7 output frequency;  
8 processing the PLL output to generate a counter output;  
9 comparing the PLL output to a first voltage level and a second voltage level;  
10 generating a voltage output based upon the compared PLL output, the voltage  
11 output having a voltage level being within a predetermined voltage range;  
12 coarse tuning the output frequency signal to the reference frequency signal based  
13 upon the voltage range;  
14 receiving a lock detection (LD) signal; [and]

controlling the counter output to cause the output frequency to be within a  
predetermined range of frequencies; and  
fine tuning the output frequency signal to the reference frequency signal, wherein  
the output frequency is tuned to the reference frequency included in a wide range  
of frequencies.

Claim 20 (currently amended): A phase control loop circuit for tuning to a reference  
frequency signal comprising:  
means for receiving the reference frequency signal having a reference frequency;  
means for generating a voltage control oscillator (VCO) output;  
means for generating a phase lock loop (PLL) output;  
means for processing the VCO output to generate an output frequency signal having  
an output frequency;  
means for processing the PLL output to generate a counter output;  
means for coarse tuning the output frequency signal to the reference frequency signal;  
means for receiving a lock detection (LD) signal; and  
means for controlling the counter output to cause the output frequency to be within a  
predetermined range of frequencies; and  
means for fine tuning the output frequency signal to the reference frequency signal,  
wherein the output frequency is tuned to the reference frequency included in a wide  
range of frequencies further including a phase-frequency detector (PFD) circuit for  
comparing said output frequency with said reference frequency to generate a PFD



17 output, said PFD output including a  $\Delta f$  signal for representing the difference between  
18 said output frequency and said reference frequency, said PLL circuit further including  
19 a charge pump (CP) circuit responsive to said PFD output for generating a current, the  
20 value of said current being based on the value of said  $\Delta f$  signal, wherein said PLL  
21 circuit further includes a loop filter responsive to said current for converting the same  
22 to generate a control voltage ( $V_{ctrl}$ ) signal having a voltage value  $V_{ctrl}$ , said  $V_{ctrl}$  signal  
23 being provided to said VCO to control said VCO output, said  $V_{ctrl}$  signal controlling  
24 said VCO output to enable said PLL circuit to fine tune said output frequency to said  
25 reference frequency, further wherein said coarse tuning circuit includes a comparator  
26 circuit, said comparator circuit including a first comparator and a second comparator,  
27 said  $V_{ctrl}$  signal being included in said PLL output, said first and second comparators  
28 being responsive to said PLL output, said first comparator being responsive to a first  
29 fixed value signal having a first voltage value, said second comparator being  
30 responsive to a second fixed value signal having a second voltage value.

1 Claim 21 (new): A phase control loop circuit for tuning to a reference frequency  
2 signal comprising:

3 a phase lock loop (PLL) circuit being responsive to a reference frequency  
4 signal having a reference frequency, said PLL circuit including a voltage  
5 control oscillator (VCO) for generating a VCO output, said PLL circuit for  
6 generating a PLL output, said phase control loop circuit processing said VCO  
7 output to generate an output frequency signal having an output frequency; and

8 a coarse tuning circuit being coupled to said PLL circuit, said coarse tuning  
9 circuit being responsive to said PLL output for processing the same to generate  
10 a counter output, said VCO being responsive to said counter output, said  
11 counter output being used for coarse tuning said output frequency signal to  
12 said reference frequency signal, said coarse tuning circuit including a first  
13 comparator responsive to the PLL output and to a first voltage level and  
14 including a second comparator responsive to the PLL output and to a second  
15 voltage level, the first and second voltage level defining a predetermined  
16 voltage range, said first comparator comparing the PLL output to the first  
17 voltage level generating a first comparator output, said second comparator  
18 comparing the PLL output to the second voltage level generating a second  
19 comparator output, said coarse tuning circuit further including a counter  
20 responsive to the first and second comparator outputs for use by the PLL  
21 causing said output frequency to be within a predetermined range of  
22 frequencies including said reference frequency by the counter stepping up or  
23 down based upon the first and second outputs to adjust the PLL output to be  
24 within the predetermined voltage range, said PLL circuit for fine tuning said  
25 output frequency signal to said reference frequency signal,  
26 wherein said PLL circuit and said coarse tuning circuit tune the output frequency to the  
27 reference frequency included in a wide range of frequencies.

1 Claim 22 (new): A phase control loop circuit as recited in claim 21 wherein said PLL  
2 circuit includes a phase-frequency detector (PFD) circuit for comparing said output  
3 frequency with said reference frequency to generate a PFD output, said PFD output

4 including a  $\Delta f$  signal for representing the difference between said output frequency  
5 and said reference frequency.

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1 Claim 23 (new): A phase control loop circuit as recited in claim 22 wherein said  
2 PLL circuit further includes a charge pump (CP) circuit responsive to said PFD  
3 output for generating a current, the value of said current being based on the value  
4 of said  $\Delta f$  signal.

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1 Claim 24 (new): A phase control loop circuit as recited in claim 23 wherein said PLL  
2 circuit further includes a loop filter responsive to said current for converting the same  
3 to generate a control voltage ( $V_{ctrl}$ ) signal having a voltage value  $V_{ctrl}$ , said  $V_{ctrl}$  signal  
4 being provided to said VCO to control said VCO output, said  $V_{ctrl}$  signal controlling  
5 said VCO output to enable said PLL circuit to fine tune said output frequency to said  
6 reference frequency.